

**AMENDMENTS TO THE CLAIMS**

This listing of claims replaces all prior listing of claims in this application.

Claims 1-38 (canceled).

39. (currently amended) A semiconductor device comprising:

a substrate; and

at least one electro-mechanically polished metal layer formed over said substrate, ~~wherein said the electro-mechanically polished metal layer containing no hardening-additive~~ layer's surface has been electro-mechanically polished against a second surface while submersed in an electrolytic bath.

40. (original) The semiconductor device of claim 39, wherein said metal layer comprises at least one metal selected from the group consisting of noble metals, noble metal alloys, refractory metals, and refractory metal alloys.

41. (original) The semiconductor device of claim 39, wherein said device comprises a capacitor with at least one electro-mechanical polished metal layer.

42. (original) The semiconductor device of claim 41, wherein said electro-mechanical polished metal layer is a bottom electrode of said capacitor.

43. (currently amended) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one

electrode surface comprises an electro-mechanically polished surface ~~containing no hardening additive~~ that has been electro-mechanically polished against a second surface while submersed in an electrolytic bath.

44. (original) The capacitor of claim 43, wherein said capacitor is a MIM capacitor.

45. (original) The capacitor of claim 43, wherein at least one electrode comprises a metal selected from the group consisting of noble metals, noble metal alloys, refractory metals, and refractory metal alloys.

46. (original) The capacitor of claim 43, wherein said at least one electrode surface is a surface of said bottom electrode.

47. (previously amended) The capacitor of claim 43, wherein the bottom electrode consists of platinum.

48. (currently amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished layer ~~containing no hardening additive~~ that has been electro-mechanically polished against a second surface while submersed in an electrolytic bath.

49. (currently amended) A semiconductor device comprising:

a substrate; and

at least one electro-mechanically polished metal layer consisting of a noble

metal formed over said substrate that has been electro-mechanically polished against a second surface while submersed in an electrolytic bath.

50. (currently amended) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an electro-mechanically polished metal surface consisting of a noble metal that has been electro-mechanically polished against a second surface while submersed in an electrolytic bath.

51. (currently amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished metal layer consisting of a noble metal provided over said substrate that has been electro-mechanically polished against a second surface while submersed in an electrolytic bath.